WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate; and

a plurality of transistors formed on said substrate to be operated by a voltage generated by a same power source, each of said transistors having a gate dielectric layer, and said plurality of transistors including transistors thickness of which is different from each other,

wherein one of said plurality of transistors that has the thinnest gate dielectric layer is selected to serve as a power source protection element.

2. The semiconductor device as set forth in Claim 1, wherein a threshold voltage of said transistor selected to serve as the power source protection element is set higher than a threshold voltage of a transistor that has a gate dielectric layer thickness of which is same as said selected transistor or thinner than the rest of said plurality of transistors other than said selected transistor.

3. The semiconductor device as set forth in Claim 1, wherein said plurality of transistors are manufactured through a multi-oxide process for forming two or more gate dielectric layers each having a different film thickness, and said plurality of transistors include at least three types of transistors each having different combinations of thickness of the gate dielectric layer and threshold voltage from each other.

4. The semiconductor device as set forth in Claim 2, wherein said plurality of transistors are manufactured through a

multi-oxide process for forming two or more gate dielectric layers each having a different film thickness, and said plurality of transistors include at least three types of transistors each having different combinations of thickness of the gate dielectric layer and threshold voltage from each other.

5. The semiconductor device as set forth in Claim1, wherein said plurality of transistors are disposed in an internal circuit surrounded by an I/O port.

6. The semiconductor device as set forth in Claim 1, wherein said plurality of transistors include a high speed processing type transistor and a low power consumption type transistor, and said transistor selected to serve as the power source protection element has higher threshold voltage than that of said high speed processing type transistor.

7. The semiconductor device as set forth in Claim 1, wherein said plurality of transistors include a high speed processing type transistor and a low power consumption type transistor, and said transistor selected to serve as the power source protection element has a dielectric layer thickness of which is same as or thinner than that of said high speed processing type transistor.

8. The semiconductor device as set forth in Claim 1, wherein said plurality of transistors include a high speed processing type transistor and a low power consumption type transistor, and leak current of said transistor selected to serve as the power source protection element is smaller than that of said high speed processing type transistor.

9. The semiconductor device as set forth in Claim 1, wherein

said plurality of transistors include a high speed processing type transistor and a low power consumption type transistor, said transistor selected to serve as the power source protection element has higher threshold voltage than that of said high speed processing type transistor, and said transistor selected to serve as the power source protection element has a dielectric layer thickness of which is same as or thinner than that of said high speed processing type transistor.

10. The semiconductor device as set forth in Claim 9, wherein said plurality of transistors are disposed in an internal circuit surrounded by an I/O port.

11. Manufacturing method of a semiconductor device, comprising the step of forming an internal circuit including a plurality of transistor groups each having a gate dielectric layer of an independently set film thickness on a substrate, wherein one of said transistors is formed as a power source protection element during said step of forming said internal circuit without performing an additional process.

12. The manufacturing method as set forth in Claim 11, wherein one of said transistors that has the thinnest gate dielectric layer is formed as the power source protection element.

13. The manufacturing method as set forth in Claim 11, wherein said step of forming said internal circuit includes forming gate dielectric layers of said power source protection element and at least one of said transistors at a same time; and a channel dosage for said power source protection element is more than a channel dosage for said at least one of said transistors.

14. The manufacturing method as set forth in Claim 12, wherein said step of forming said internal circuit includes forming gate dielectric layers of said power source protection element and at least one of said transistors at a same time; and a channel dosage for said power source protection element is more than a channel dosage for said at least one of said transistors.

15. The manufacturing method as set forth in Claim 11, wherein said channel dosage for said power source protection element is equal to a total channel dosage for at least two of said transistors included in said internal circuit.

16. The manufacturing method as set forth in Claim 12, wherein said channel dosage for said power source protection element is equal to a total channel dosage for at least two of said transistors included in said internal circuit.

17. The manufacturing method as set forth in Claim 11, wherein said step of forming said internal circuit includes:

performing a first impurity ion implantation into a first forming region of a first transistor other than said power source protection element included in said transistors; and

performing a second impurity ion implantation into a second forming region of a second transistor other than said power source protection element or said first transistor included in said transistors;

wherein said first impurity ion implantation and said second impurity ion implantation are performed into a region of said power source protection element for adjusting a threshold voltage of said power source protection element.

18. The manufacturing method as set forth in Claim 12, wherein said step of forming said internal circuit includes:

performing a first impurity ion implantation into a first forming region of a first transistor other than said power source protection element included in said transistors; and

performing a second impurity ion implantation into a second forming region of a second transistor other than said power source protection element or said first transistor included in said transistors;

wherein said first impurity ion implantation and said second impurity ion implantation are performed into a region of said power source protection element for adjusting a threshold voltage of said power source protection element.